WHAT IS CLAIMED IS:

1. Manufacturing method of a semiconductor device comprising the steps of:

forming a dielectric layer on a semiconductor substrate;

forming a recess on said dielectric layer;

forming a first metal layer so as to fill a portion of said recess;

forming a second metal layer on said first metal layer so as to fill the remaining portion of said recess; and

performing heat treatment of said first metal layer and said second metal layer.

2. The manufacturing method as set forth in Claim 1, wherein said second metal layer contains a metal that is the main constituent of said first layer and at least one dissimilar element different from such metal.

3. The manufacturing method as set forth in Claim 1, further comprising the step of removing said first metal layer and said second metal layer formed outside said recess.

4. The manufacturing method as set forth in Claim 1, wherein a surface of said first metal layer and that of said second metal layer are formed in a generally uniform orientation through said heat treatment process.

5. The manufacturing method as set forth in Claim 1, wherein said first metal layer and said second metal layer are formed in an average grain size of not less than 1 μm through said heat treatment process.

6. The manufacturing method as set forth in Claim 1, wherein

a surface of said first metal layer and that of said second metal layer are formed in an orientation of (200) through said heat treatment process.

7. Manufacturing method of a semiconductor device comprising the steps of:

forming a first metal layer on a semiconductor substrate;

forming over the first metal layer a second metal layer containing a metal that is said main constituent of said first metal layer and a dissimilar element different from such metal; and

performing heat treatment of said first metal layer and said second metal layer to form a dissimilar element-diffused metal layer, a surface whereof has a generally uniform orientation.

8. Manufacturing method of a semiconductor device comprising the steps of:

forming a first metal layer on a substrate;

forming over said first metal layer a second metal layer containing a metal that is the main constituent of said first metal layer and a dissimilar element different from such metal; and

performing heat treatment of said first metal layer and said second metal layer to form a dissimilar element-diffused metal layer, having an average grain size of not less than 1μm.

9. The manufacturing method as set forth in Claim 1, wherein said surface of said dissimilar element-diffused metal layer attains an orientation of (200) through said step of forming said dissimilar element-diffused metal layer.

10. The manufacturing method as set forth in Claim 7, wherein said surface of said dissimilar element-diffused metal layer

attains an orientation of (200) through said step of forming said dissimilar element-diffused metal layer.

11. The manufacturing method as set forth in Claim 8, wherein said surface of said dissimilar element-diffused metal layer attains an orientation of (200) through said step of forming said dissimilar element-diffused metal layer.

12. Manufacturing method of a semiconductor device comprising the steps of:

forming a dielectric layer on a semiconductor substrate;

forming on said dielectric layer a first interconnect trench and a second interconnect trench narrower than said first interconnect trench;

forming a first metal layer so as to fill a part of an inner portion of said first interconnect trench and an entire inner portion of said second interconnect trench; and

forming a second metal layer over said first metal layer so as to also fill the remaining part of said inner portion of said first interconnect trench.

13. The manufacturing method as set forth in Claim 12, further comprising the step of performing heat treatment of said first metal layer and said second metal layer.

14. The manufacturing method as set forth in Claim 12, wherein said second metal layer contains a dissimilar element different from a metal that is the main constituent of said first metal layer.

15. The manufacturing method as set forth in Claim 1, wherein a thickness of said second metal layer at a plain portion thereof

is made greater than a thickness of said first metal layer at a plain portion thereof.

16. The manufacturing method as set forth in Claim 12, wherein a thickness of said second metal layer at a plain portion thereof is made greater than a thickness of said first metal layer at a plain portion thereof.

17. The manufacturing method as set forth in Claim 1, wherein plating method is employed for forming said first metal layer, in said step of forming said first metal layer.

18. The manufacturing method as set forth in Claim 7, wherein plating method is employed for forming said first metal layer, in said step of forming said first metal layer.

19. The manufacturing method as set forth in Claim 8, wherein plating method is employed for forming said first metal layer, in said step of forming said first metal layer.

20. The manufacturing method as set forth in Claim 12, wherein plating method is employed for forming said first metal layer, in said step of forming said first metal layer.

21. The manufacturing method as set forth in Claim 1, wherein said step of forming said first metal layer further comprises the steps of:

forming on said semiconductor substrate by sputtering a seed metal layer containing a metal that is the main constituent of said first metal layer and said dissimilar element; and

forming by plating a plated metal layer containing said metal that is the main constituent of said first metal layer so as to cover said seed metal layer.

22. The manufacturing method as set forth in Claim 7, wherein said step of forming said first metal layer further comprises the steps of:

forming on said semiconductor substrate by sputtering a seed metal layer containing a metal that is the main constituent of said first metal layer and said dissimilar element; and

forming by plating a plated metal layer containing said metal that is the main constituent of said first metal layer so as to cover said seed metal layer.

23. The manufacturing method as set forth in Claim 8, wherein said step of forming said first metal layer further comprises the steps of:

forming on said semiconductor substrate by sputtering a seed metal layer containing a metal that is the main constituent of said first metal layer and said dissimilar element; and

forming by plating a plated metal layer containing said metal that is the main constituent of said first metal layer so as to cover said seed metal layer.

24. The manufacturing method as set forth in Claim 12, wherein said step of forming said first metal layer further comprises the steps of:

forming on said semiconductor substrate by sputtering a seed metal layer containing a metal that is the main constituent of said first metal layer and said dissimilar element; and

forming by plating a plated metal layer containing said metal that is the main constituent of said first metal layer so as to cover said seed metal layer.

25. The manufacturing method as set forth in Claim 1, wherein sputtering method is employed for forming said second metal layer, in said step of forming said second metal layer.

26. The manufacturing method as set forth in Claim 7, wherein sputtering method is employed for forming said second metal layer, in said step of forming said second metal layer.

27. The manufacturing method as set forth in Claim 8, wherein sputtering method is employed for forming said second metal layer, in said step of forming said second metal layer.

28. The manufacturing method as set forth in Claim 12, wherein sputtering method is employed for forming said second metal layer, in said step of forming said second metal layer.

29. The manufacturing method as set forth in Claim 1, wherein bias sputtering method for applying a bias to said semiconductor substrate is employed for forming said second metal layer, in said step of forming said second metal layer.

30. The manufacturing method as set forth in Claim 7, wherein bias sputtering method for applying a bias to said semiconductor substrate is employed for forming said second metal layer, in said step of forming said second metal layer.

31. The manufacturing method as set forth in Claim 8, wherein bias sputtering method for applying a bias to said semiconductor substrate is employed for forming said second metal layer, in said step of forming said second metal layer.

32. The manufacturing method as set forth in Claim 12, wherein bias sputtering method for applying a bias to said semiconductor substrate is employed for forming said second metal

layer, in said step of forming said second metal layer.

33. The manufacturing method as set forth in Claim 1, wherein said first metal layer mainly contains copper.

34. The manufacturing method as set forth in Claim 12, wherein said first metal layer mainly contains copper.

35. A semiconductor device comprising:

a semiconductor substrate; and

a dissimilar element-diffused metal layer formed on said semiconductor substrate, containing copper and a dissimilar element other than copper and having a generally uniform orientation at a surface thereof.

36. A semiconductor device comprising:

a semiconductor substrate; and

a dissimilar element-diffused metal layer formed on said semiconductor substrate, containing copper and a dissimilar element other than copper, constituted of grains of an average size not less than 1 μm.

37. The semiconductor device as set forth in Claim 35, wherein an average grain size of crystals of said dissimilar element-diffused metal layer is greater than an average thickness of said dissimilar element-diffused metal layer.

38. The semiconductor device as set forth in Claim 36, wherein an average grain size of crystals of said dissimilar element-diffused metal layer is greater than an average thickness of said dissimilar element-diffused metal layer.

39. The semiconductor device as set forth in Claim 35, wherein a surface of said dissimilar element-diffused metal layer

has an orientation of (200).

40. The semiconductor device as set forth in Claim 36, wherein a surface of said dissimilar element-diffused metal layer has an orientation of (200).

41. The semiconductor device as set forth in Claim 35, wherein said dissimilar element-diffused metal layer constitutes an interconnect, a plug or a pad.

42. The semiconductor device as set forth in Claim 36, wherein said dissimilar element-diffused metal layer constitutes an interconnect, a plug or a pad.

43. The semiconductor device as set forth in Claim 35, wherein said dissimilar element-diffused metal layer is formed by plating.

44. The semiconductor device as set forth in Claim 36, wherein said dissimilar element-diffused metal layer is formed by plating.

45. A semiconductor device comprising:

a semiconductor substrate;

a first interconnect formed on said semiconductor substrate; and

a second interconnect constituted of a metal that is the main constituent of said first interconnect, formed in the identical interconnect layer; wherein

said second interconnect is narrower than said first interconnect; and

said first interconnect and said second interconnect have a different orientation at the respective surfaces thereof.

46. The semiconductor device as set forth in Claim 45, wherein a width of said second interconnect is narrower than that of said first interconnect, and a surface of said first interconnect has a principal orientation of (200), and said second interconnect has that of (111). A width of said first interconnect can be made for example not less than 1 μm, and that of said second interconnect not more than 1 μm.

47. A semiconductor device comprising:

a semiconductor substrate;

a first interconnect formed on said semiconductor substrate; and

a second interconnect constituted of a metal that is the main constituent of said first interconnect, formed in the identical interconnect layer; wherein

said second interconnect is narrower than said first interconnect;

said first interconnect contains a dissimilar element other than a main constituent of said first interconnect diffused throughout said first interconnect; and

said second interconnect contains a dissimilar element formed over an upper surface thereof.

48. A metal interconnect constituted of a plated metal layer comprising a plurality of dissimilar elements, wherein an average size of grains contained in said plated metal layer is not less than 1 μm.

49. A metal interconnect constituted of a plated metal layer comprising a plurality of dissimilar elements, wherein said plated

metal layer is constituted of a single grain.

50. The metal interconnect as set forth in Claim 48, having a width not less than 1 μm.

51. The metal interconnect as set forth in Claim 49, having a width not less than 1 μm.